Remarks

This communication is in response to the Office Action of March 9, 2006. In the Office Action, claims 20-28 were rejected.

Claims 20 through 28 are pending in the application. Claims 20 through 27 were rejected. Claims 20-22, 24, 26 and 27 are amended. It is submitted that the amendments to the claims address the claim rejections without adding new matter.

Claim 29 is canceled.

The claim rejections are respectfully traversed because the cited art, alone or in combination, fails to disclose or suggest the recitations of at least independent claim 20. In particular, the cited art fails to disclose or suggest "determining desired changes in the metal one layer needed to implement the modifications in logic design, including connecting the at least one programmable circuit to the plurality of circuits; and forming a metal one layer on said semi-fabricated semiconductor wafer different from the metal one layer of the original specimen to effect the desired changes."

Amendments to the Specification

The Abstract was objected to as having the phrase "The Abstract and, . . . MPEP 608.01(b)". The objection to the abstract is traversed. However, in order to advance prosecution, the abstract has been amended. The amendment to the specification does not add new matter.

Claim Objection

Claim 20 was objected to the phrase "the manufacturing" should be changed to –a manufacturing--, in order to minor informality. The objection to claim 20 is traversed. However, in order to advance prosecution, claim 20 has been amended.

Claim Rejections under 35 U.S.C. § 112, first paragraph

Claim 20 was rejected under 35 U.S.C. § 112, first paragraph. The § 112, first paragraph rejection is traversed. However, to advance prosecution claims 20-22, 24, 26 and 27 are amended.

In view of the claim amendments, it is believed that the § 112, first paragraph rejection is obviated. Support for the claim amendments can be found at least in the specification at page 11, line 20, for the claim recitation of providing a partially-fabricated semiconductor wafer that lacks a metal one layer, because the partially-fabricated wafer is "left unfinished before the 'metal one stage.'" For the recitation related to examining an original specimen, support can be found in the specification at page 11, line 10 et seq.

Double Patenting Rejection

Claims 20 through 27 are rejected under the Judicially Created Doctrine of Obviousness-Type Double Patenting as being unpatentable over claims 1 through 10 of U.S. Patent No. 6,601,228 and claims 1 through 13 of U.S. Patent No. 6,209,118.

Accompanied with this paper are two terminal disclaimers for U.S. Patent No. 6,601,228 and U.S. Patent No. 6,209,118. It is believed that the terminal disclaimers are in compliance with 37 C.F.R. 1.321(c), and therefore withdrawal of the double patenting rejection is requested.

Rejections under 35 U.S.C. § 102

Claims 20, 21, 24 and 27 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. Fudanuki et al. (hereinafter "Fudanuki"). Fudanuki fails to disclose the recitations of at least independent claim 20 for at least the following reasons.

Fudanuki discloses a semiconductor integrated circuit with mixed gate array and standard cell. Fudanuki states:

> the second feature of the present invention resides in that a logic circuit area (a logic block) having mixed standard cell and gate array layout and a megacell (and/or a megafunction) are provided on a same semiconductor chip (LSI chip). Where the term "megacell" means the cell which has fixed layout pattern of the cell, and the representative megacell is memory such as ROM or RAM, multiplier, etc. whose performance depends on the layout. The term "megafunction" means the circuit which can be implemented by combination of macrocells on the layout though it is treated theoretically as a lump of cells, and

> the representative megafunction is ALU, CPU core, etc. whose chip integration degree is affected by connection relationship between the megafunction and other blocks.

Fudanuki, col. 4, lines 50-62. From above, it is understood that portions of the logic circuit area include modifiable areas: the standard cell and gate array layout ("which have no logic function by themselves," Fudanuki, col. 2, lines 18-20); and include a "fixed," non-modifiable areas: the megacell and/or a megafunction (a lump of cells).

Further, according to Fudanuki,

> the gate array basic cells GC are arranged preliminarily in the empty spaces in which the standard cells SC are not arranged in the logic block 231, and the circuit change is made by use of the basic cells GC.

Fudanuki, col. 13, lines 31-37.

With respect to gate array basic cells that are added to empty spaces where standard cells are not arranged, "*basic cells used in the gate array approach are identical cells which have no logic function by themselves*." Fundanuki, col. 2, lines 18-20. Accordingly, the gate array basic cell is not a programmable circuit.

Because the modifiable portions of the LSI chip 1 from the second embodiment of Fundanuki (col. 13) are only modifiable in areas containing gate array basic cells and standard cells, which have no logic function by themselves (i.e. which are not programmable circuits), Fundanuki fails to disclose "determining desired changes in the metal one layer needed to implement the modifications in *logic design*, including connecting the at least one programmable circuit to the plurality of circuits; and forming a metal one layer on said partially-fabricated semiconductor wafer different from the metal one layer of the original specimen to effect the desired changes."

Reconsideration and withdrawal of the § 102(e) rejection is requested.

Claim rejections under 35 U.S.C. § 103

Claims 22, 23, 25 and 26 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Fudanuki et al. in view of U.S. Patent No. 5,787,012 Levitt.

Levitt fails to remedy the deficiencies of Fundanuki because the integrated circuit in Levitt includes "layer identification signal writing circuitry" and their requisite connections to

produce "circuit identification signals." Because the signal writing circuitry performs a single function, the production of circuit identification signals, Levitt fails to disclose the programmable circuit of the present invention because according to claim 20, a programmable circuit is "capable of performing at least one of a plurality of logic transfer functions upon programming." As a result, because Levitt fails to disclose the programmable circuit of the present invention, Levitt also fails to disclose or suggest "determining desired changes in the metal one layer needed to implement the modifications in logic design, including connecting the at least one programmable circuit to the plurality of circuits; and forming a metal one layer on said semi-fabricated semiconductor wafer different from the metal one layer of the original specimen to effect the desired changes."

Reconsideration and withdrawal of the § 103 rejection is requested because the cited references, when viewed alone or in combination, fail to disclose or suggest at least the requirements of independent claim 20.

Dependent claims

Dependent claims 21-27 depend from independent claim 20, and further recite additional novel aspects. Therefore, it is believed that claims 21-27 are distinguishable over the cited art for at least the reasons set forth above.

CONCLUSION

It is believed that no additional fees have been incurred in filing this paper. However, two terminal disclaimers accompany this paper, and a check for appropriate is included herewith. The Commissioner is also hereby authorized to credit any overages or charge any deficiencies to Deposit Account No. 04-1420.

In view of the above, Applicant respectfully submits that the present application is in condition for allowance. Reconsideration of the present application and a favorable response are respectfully requested.

This application now stands in allowable form, and reconsideration and allowance are respectfully requested.

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